•	Application No.	Applicant(s)
Madian at Allan at 114	10/719,265	SIM ET AL.
Notice of Allowability	Examiner	Art Unit
	David Lam	2827
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to		
2. The allowed claim(s) is/are <u>1-30</u> .		
3. The drawings filed on <u>21 November 2003</u> are accepted by the Examiner.		
4.		
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. Interview Summary Paper No./Mail Da 7. Examiner's Amendr	te .

U.S. Patent and Trademark Office PTOL-37 (Rev. 1-04) PRIMARY EXAMINER

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Allowable Subject Matter

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The following is an examiner's statement of reasons for allowance: Claims 1-30 are 1. allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach: a semiconductor memory device comprising: n dummy memory cells, among others as claimed in independent claim 1, being operative to draw current from a source line responsive to complement of n bit data word, wherein the total number of memory cells drawing from the source line is n; a dummy memory cell circuit, among others as claimed in independent claim 5, operative to draw current from the source line responsive to the n bit data word such that the total current drawn by the memory cell and the dummy cell circuit during a program operation is given by n* a current drawn by one of the n memory cells; n/y dummy memory cells, among others as claimed in independent claim 10, being operative to drawn current from the source line responsive to the n bit data word such that respective currents drawn by respective one of the n/y dummy memory cells ranges from approximately zero to y* a current drawn by one of the n memory cells; a bias current, among others as claimed in independent claims 17, 18, flow from the source line to at least one or more dummy bit line lines in response to the n input data during a program operation. Method of operating/programming the memory device comprising step of applying n programming voltages to n memory cells so as to cause the memory cells to draw current flow from the source line, and among others as claimed in independent claim 15; during programming operation, generating a bias current flowing from the selected source line to at least one or more dummy bit line in response to the n input data, and among others as claimed in independent claim 30.

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Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

- 2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- Yeh et al. (6,785,163) disclose a trim circuit and method for tuning a current level of a reference cell in a flash memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

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system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Lam

March 29, 2005

DAVID LAM PRIMARY EXAMINER